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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Roman Woyzichovski

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EXAMINER

PERILLA, JASON M

ART UNIT

PAPER NUMBER

2611

MAIL DATE

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12/22/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Examiner's Remarks

1. Claims 21-42 are pending in the instant application.

Response to Amendment/Argument

2. The Applicant's remarks, filed December 4, 2008, have been considered by the Examiner.

In view of the Applicant's amendment to claim 29, for purposes of appeal, the rejections in the final office action of September 5, 2008 under 35 U.S.C. § 112, second paragraph, will be withdrawn.

The Applicant has presented the following arguments against the Liessner (U.S. Pat. No. 5079549) in view of Garverick et al (U.S. Pat. No. 5134578; "Garverick") prior art combination's application to the claims: (1) the combination does not support a fully digital implementation of the claimed invention and requires a substantial redesign of the primary reference Liessner, and (2) Liessner does not disclose accumulating results for generating correctional values over a specifiable time interval.

Regarding the Applicant's argument (1), as applied in the combination of Liessner in view of Garverick presented in the previous office actions and below, the combination results in a digital implementation of many of Liessner's original analog components. The Applicant's suggestion that such a "redesign" from an analog to a digital embodiment would "change the basic principal under which the device described by Liessner was designed to operate" (6/2/08 remarks, pg. 9) is not persuasive. Rather, Liessner's "basic principal" of operation would be maintained in a fully digital implementation as would be readily understood by one having ordinary skill in the art.

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As is notoriously known and understood in the art, properly designed digital implementations provide for zero loss in signal integrity as compared to analog ones. Moreover, the conversion of Liessner's analog components to digital ones would involve merely a routine level of skill in the art and would produce only expected and predictable results.

Regarding the Applicant's argument (2), the accumulation of UP and DOWN outputs (via fig. 4A, refs. 25 and 27) from Liessner's the error signal detector (fig. 4A, ref. 22) is performed over a specifiable time interval because it is limited by the disable pulse generator (fig. 4A, ref. 29). As broadly as claimed, even if the disable pulse generator 29 merely prevents the outputs of the UP (25) and DOWN (27) count generators from being updated to the SIN and COS lookup tables, it yet causes their respective accumulation outputs "UP COUNT" and "DOWN COUNT" to be "specifiable" as claimed. Therefore, their "accumulations" are specifiable.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Jason M Perilla/
Art Unit 2611
December 16, 2008

/jmp/

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611